International Journal of Advanced Research in Technology and Management Sciences (IJARTMS)
ISSN (Online): XXXX-XXXX
Volume 1, Issue 2, pp 6-10, November-2021

Implementation of Contemplation Of Synchronous Gray Code Counter Using Reversible Logic Gates.

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Abstract **-** A Gray Code is an encoding of integers as sequences of bits with the property that the representations of adjacent integers differ in exactly one binary position. Gray Codes have many practical applications that go beyond research interests. There are different types of gray codes: Binary reflected, Maximum Gap, Balanced, Antipodal and Non Composite to name a few. On the other hand Reversible logic has received great attention due to their ability to reduce the power dissipation--an important aspect of low power circuit design. Other applications include Optical information processing, DNA computing, bio informatics, quantum computation and nanotechnology. Counters have a primary function of producing a specified output sequence and are thus sometimes referred to as pattern generators. This paper proposes design of different gray code counters using reversible logic gates, to draw comparative conclusions upon their performance.

Keywords: Gray Codes, Binary reflected, Maximum Gap, Balanced, Antipodal and Non Composite.

I. INTRODUCTION

The power consumption which leads to heat dissipation in computer machinery has become one of the greatest challenge and research interest today. Any computation that can be reversibly performed both logically and thermodynamically, leads to dissipating arbitrarily little energy. R.Landauer in1961 showed that irreversibility in the computing process that leads to loss of information requires minimum heat generation in the order of k*T for each irreversible function, k is Boltzmann's constant and T is the absolute temperature. C.H.Bennett in 1973 showed that an irreversible computer can always be made reversible. Reversible logic circuits naturally take care of heating since in a reversible logic every input vector can be uniquely recovered from its output vectors and therefore no information is lost. According to zero energy dissipation would be possible only if the network consists of reversible gates. Any reversible gate performs the permutation of its input vector patterns only. If a reversible gate has k inputs, and therefore k outputs, then we call it a k*k reversible gate.

Additional outputs added so as to make the number of inputs and outputs equal which are not used in the synthesis of a given function but sometimes mandatory to achieve reversibility are called garbage. The important design constraints for reversible logic circuits are: Reversible logic gates do not allow fan-outs. Reversible logic circuits should have minimum quantum cost. The design can be optimized so as to produce minimum number of garbage outputs. The reversible logic circuits must use minimum number of constant inputs. The remainder of this paper is organized as follows –Section II gives a quick run through the different reversible logic gates used in this paper. Section III lists the different types of gray codes and the codes itself in a lexicographical order. Section IV shows the design of reversible gray code counter for the different gray codes enlisted in the section III and performs a comparative study.

II. LITERATURE SURVEY

In 1961, R.Landauer stated that in irreversible logic computation heat dissipates due to Loss of information bits. Each bit of information dissipates kTIn2 amount of heat, where k is the Boltzmann constant and T is the absolute temperature. In 1973, C.H.Bennett stated that this heat dissipation problem can be solved by using reversible computation. Reversible computing follows the property of reversibility in which there is one to one mapping between the input and output vectors. A circuit is set to be reversible if the input vectors can be distinctively retrieved from the output vectors

3.1 SURVEY

[1]In 2010, Lihui Ni et.al presented a general method of constructing the reversible full adder. A range of reversible full adders with only two reversible gates and two garbage outputs were realized using this approach. This approach had progress in the gate count, garbage count and quantum cost.

[2]In 2011, Nagapavani et.al presented a paper that proposed a design of a reversible 4-bit shift registers which were compared with previous design. For this proposed designs Reversible edge triggered D flip-flop such as SISO, SIPO, PISO and PIPO. These designs have the applications to perform serial-to-parallel and parallel-to-serial conversions.

[3] In 2011, Zhijin Guan et.al presented a design of Arithmetic Logic Unit based on reversible logic gates. This paper presents that the minimum number of information

bits were required for designing reversible Arithmetic Logic Unit. This design has low power consumption and reduces the loss by reusing information bits.

[4] In 2012, T. Naga Babu et.al presented reversible adder/subtractor circuits using reversible logic gates like DKG and TSG gate. The proposed designs were better than the previous designs in terms of hardware complexity, number of gates, garbage outputs and constant inputs.

[5] In 2012, Xueyun Cheng et.al presented a simplification algorithm for reversible logic networks of positive/ negative control gates. This algorithm can lessen the gate count as well as number of control bits. This simplified algorithm required only 8.10 average numbers of control bits and 11 gate counts.

[6] In 2013 Rakshith Saligram et.al presented a design of low logical cost adders using novel parity conserving Toffoli gate. In this design parity preserving gate had itself been used to work as a Toffoli gate. This proposed design has a slightest logical cost. This design has 22.22% enhancement for quantum cost.

[7] In 2013, Mr. M.Saravanan et.al presented a design of energy efficient code converters using reversible logic gates. This paper describes the various code converters such as grey to binary, binary to grey, BCD to excess-3 using reversible logic gates. These converters have low power consumption and higher efficiency as compared with conventional logic circuits.

[8] In 2014, Avinash G.Keskar et.al presented a design of eight bit novel reversible arithmetic and logic unit. This design can be used to realize large reversible systems. A reversible implementation of eight bit arithmetic and logic unit required less number of gates and garbage outputs.

[9] In 2014, R.Jayashree et.al proposed that flip flops such as D flip-flop, T flip-flop and JK flip-flop were designed using various previous reversible gates and their truth table were verified by simulation. These proposed designs were compared in terms of average power consumption, garbage outputs and constant inputs.

[10]In 2014, Asima Jamal et.al proposed a design of sixteen bit binary sequential counter using Feynman and Fredkin gates. The Up/Down operation of this design was controlled by the control input UP/DOWN. The control input should be 1 for UP operation and the control input should be 0 for down operation.

[11]In 2014, Ankur Sarker et.al presented a design that performs addition/ subtraction operations using parity preserving and fault tolerant reversible gates. This circuit not only reduced the number of logic gates but also reduced the quantum cost and garbage outputs. The highest improvements of the presented design were 33.33% for garbage output, 26.66% for quantum cost and 50% for gate count.

[12]In 2015, Sayyad khaja Moinuddin et.al proposed 2:4 reversible decoder using two Feynman and two Fredkin gates. The proposed reversible decoder can be used in active high as well as in active low mode of operation which depends upon the select lines. The proposed design has low quantum cost and this design can be extended to 3:8 decoders.

[13] In 2015, Md. Samiur Rahman et.al proposed an Optimized Design of Full-Subtractor Using New SRG Reversible Logic Gates and VHDL Simulation. In this proposed design SRG gate worked singly as a Full-subtractor circuit. This proposed work can be used for designing nanotechnology based large reversible systems.

[14] In 2015, Avishek Bose et.al presented a design of compact reversible online testable ripple carry adder. The main property of this design is that one input line of the adder has no control on the other input line. This design has improvement of 25% on number of gates, 42.30% on quantum cost and 50% on number of constant inputs. [15] In 2016, Umesh Kumar et.al proposed a paper that describes the performance evaluation of reversible logic gates. In this paper classical gates and quantum gates are compared on the various parameters. It is analyzed that power consumption, heat dissipation can be minimized using various reversible logic gates such as Toffoli, Fredkin and Peres gate.

[16] In 2016, Deeptha A et.al proposed a design of Reversible 8-bit ALU by cascading 1-bit ALUs. Control unit and the adder unit were the major units of 1-bit ALUs. Control Output Gate (COG) and Haghparast Navi Gate (HNG) have been used for control unit and adder unit respectively. The proposed design was compared with the previous design and has lesser propagation delay.

[17] In 2016, MojtabaValinataj et.al proposed a design of a new low-cost gate with the quantum cost of 10. This new low-cost gate was used as a parity preserving full adder with the minimum hardware complexity. Some new low-cost fault-tolerant adders are carry skip, carry look-ahead and BCD adders which are highly proficient in terms of quantum cost, total logical calculation and transistor count as compared to the previous designs.

[18] In 2017, A.V.Ananthalakshmi et.al proposed a design of Reversible floating-point square root using modified non-restoring algorithm. Non-restoring method consumed less number of logical resources and the remainder was not restored in each step. GST algorithm was used for this floating-point square root which has reduced the area and power consumption. This design is efficient in terms of number of reversible gates, constant inputs, garbage outputs and quantum cost.

[19] In 2017, A.Kamaraj et.al presented a design of Arithmetic Logic Unit using Novel reversible gates and it was evaluated in Quantum Cellular Automata. This Arithmetic Logic Unit can be used for low power applications. This design mitigates quantum cost, garbage outputs. It has improvement of 50% on constant inputs, 58.3% on gate counts and 62% on number of cells.

[20]In 2017, Dhoumendra Mandal et.al presented a design of all optical one bit binary comparator using reversible logic gates. In this design, reversible logic gates based on

frequency encoded data were used for designing one bit comparator. This comparator circuit can be used to propose all optical Arithmetic Logic Unit.

III. PROPOSED ARCHITECTURE

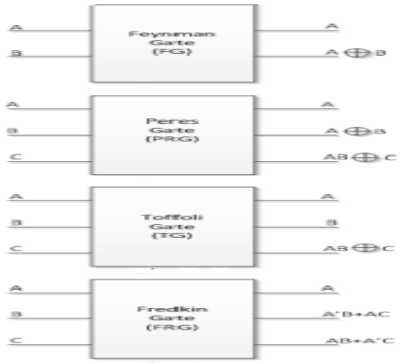


Figure 4.1:Reversible logic gates

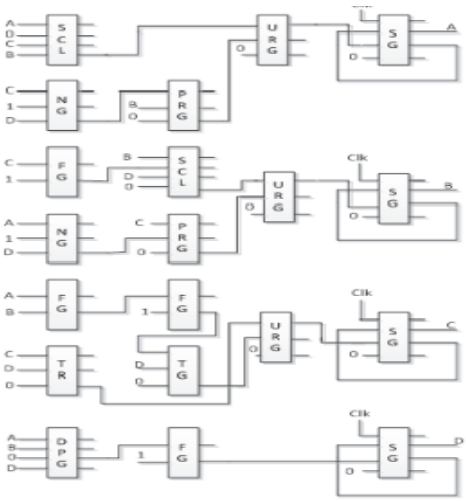


Fig: Binary reflected gray code counter

Binary Reflected Gray Codes		Antipodal Gray Codes		Uniformly Balanced Gray Codes	
0000	1100	0000	1010	0000	0110
0001	1101	0001	1011	1000	0100
0011	1111	0011	1001	1100	0101
0010	1110	0111	1101	1101	0111
0110	1010	1111	0101	1111	0011
0111	1011	1110	0100	1110	1011
0101	1001	1100	0110	1010	1001
0100	1000	1000	0010	0010	0001

Fig : Comparison of the performance metrics of the counter

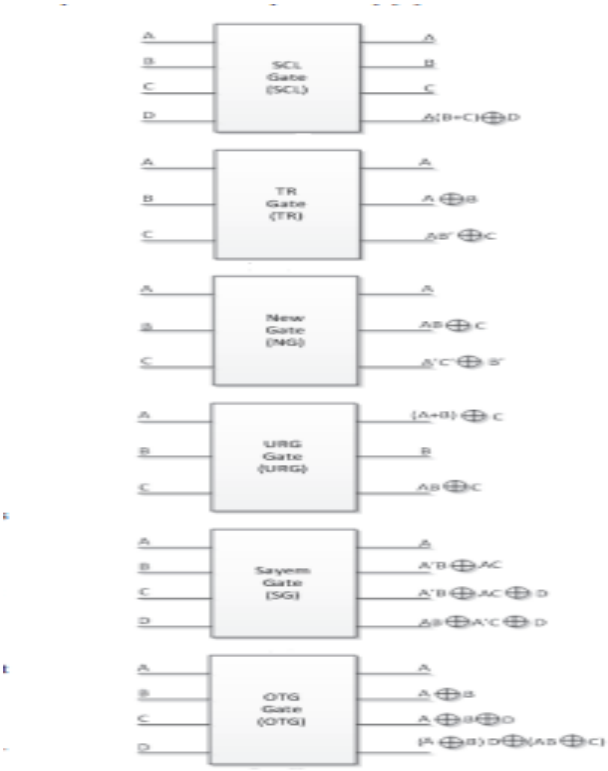


Fig: reversible logic gates continued

ADVANTAGES &APPLICATIONS

ADVANTAGES

1.Gray code counters are non-glitch counters only one bit changes.

2.It is used for synchronous FIFO'S address pointers.

3.Reduse the digital noise as compared to normal counters.

4.Used for facilitates error correction in digital communication.

5.Used to find applications in data path synchronous.

APPLICATIONS

1.Encoding and decoding digital image processing.

2.Data compression Technique.

3.Processor allocation in the hyper cube.

4.Ordering of documents on shelves.

5.Informatin storage and retrieval.

6.Circuit testing.

7.Robotics and mechanical encoding.

8.Cable TV systems.

IV. SIMULATION & SYNTHESIS RESULTS

4.1 SYNTHESIS RESULTS

4.1.1 RTL SCHEMATIC(SYNTHESIS)

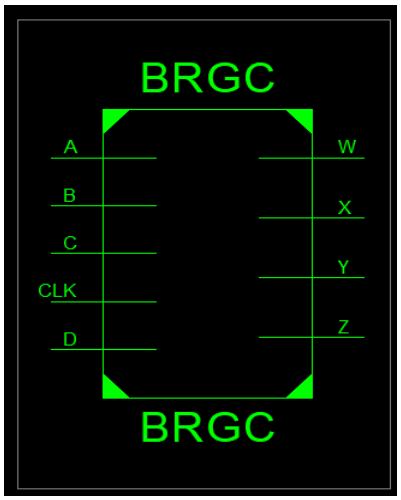


Fig: RTL view of BRGC

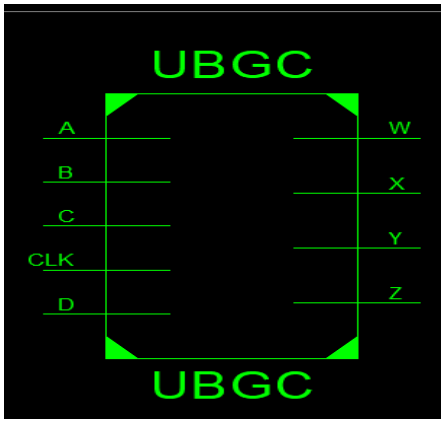
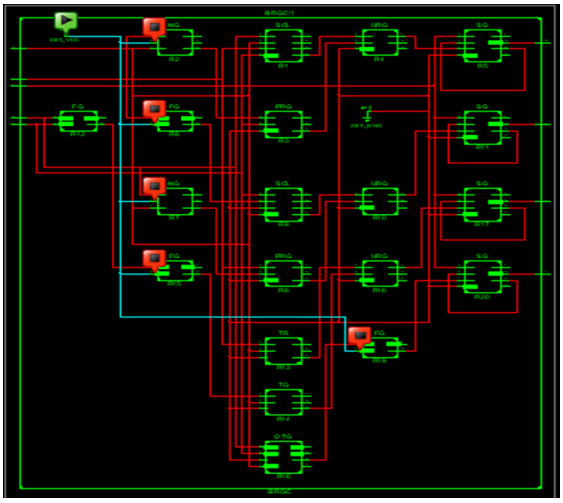
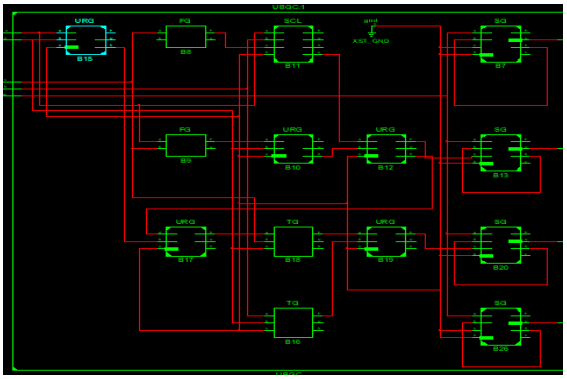


Fig RTL diagram of UBGC

4.1.2RTL SCHEMATIC





REPORT COMPARISION

Counter Name	Number of Gates	Delay
BRGC	XOR's-43 LUT's-7	1.299ns
UBGC	XOR's-31 LUT's-7	1.089ns

Table: Comparison table

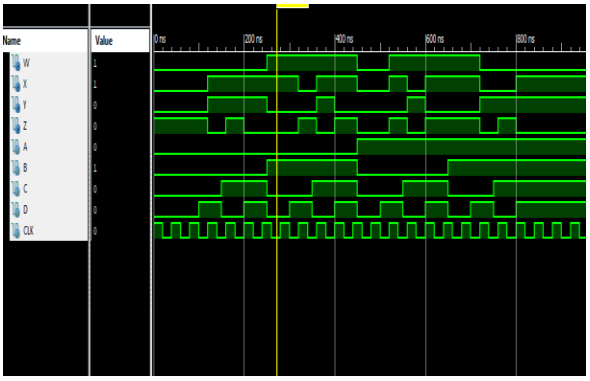


Fig: stimulation result for BRGC counter

V. CONCLUSION & FUTURE SCOPE

This paper gives a comparative study of gray code variants namely Binary reflected code counter, uniform balanced gray code counter. These variants are analyzed and number of gates and delays. The counters are simulated and verified using XILINX.

FUTURE SCOPE

Gray code counters are non glitch counters since only one bit changes. Gray code counters can be used for asynchronous FIFO's address pointers. They reduce the digital noise as compared to the normal counters .They also find application in data path synchronization .They are widely used to facilitate error correction in digital communications.

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